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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/645,875	08/25/2000	Yoshikatsu Uetake	OKI 260	4073

23995 7590 10/05/2005

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EXAMINER	
HAN, CLEMENCE S	
ART UNIT	**PAPER NUMBER**
2665	

DATE MAILED: 10/05/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/645,875	UETAKE ET AL.	
	Examiner	Art Unit	
	Clemence Han	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4,9 and 10* is/are allowed.

6)☒ Claim(s) *5-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claim 5-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Murata et al. (US 4,759,010).

Regarding to claim 5, Masuda teaches a method of switching data in a digital switching system, comprising: a multiplexing step of multiplexing time slots from a first plurality of circuits (Column 1 Line 15-18); a writing step of sequentially writing into a switching memory 20 data of the time slots multiplexed by the multiplexing step (Column 1 Line 15-18); a data interchange step comprising receiving connection information (control data D) from an upper layer controller 40, corresponding to before and after switching (Column 6 Line 45-49), writing the connection information (control data D) in a control memory 12, 13 at addresses (address signal ADR) designated by the connection information (Column 5 Line 31-34), sequentially reading out the connection information stored in the control memory 12, 13 as read-out order for the multiplexed time slot data written in the switching memory 20 (Column 6 Line 34-37), in synchronization with an internal timing standard (Column 4 Line 38-39) in response to a switching

directive (write control signal 306) from the upper layer controller 40, so as to change accommodation destinations of the multiplexed time slot data (Column 1 Line 26-30); and a demultiplexing step of demultiplexing the data from the data interchange step into a second plurality of circuits (Column 1 Line 18-22).

Regarding to claim 6, Masuda teaches wherein the data interchange step comprises: an information receiving step of receiving the connection information (control data D) from the upper layer controller 40 before switching, and the same after switching, respectively (Column 6 Line 45-49); an information input/output step of storing the connection information (control data D) received in the information receiving step (Column 5 Line 31-34), and reading out the connection information received before and after switching (Column 6 Line 34-37); a switching signal generation step of generating a switching signal (WS and SE in Column 5 Line 40-41) for switching in synchronization with the timing (Column 4 Line 38-39) in response to the switching directive (write control signal 306) of the connection information received from the upper layer controller 40; a selection step of selecting the connection information after switching all of the connection information as read out in the information input/output step in response to the switching signal generated (Column 5 Line 67 – Column 6 Line 2); and a read-out

step of reading out the multiplexed data as written in the writing step on the basis of the connection information selected in the selection step (Column 1 Line 18-30).

Regarding to claim 7, Masuda teaches wherein the data interchange step comprises: an information receiving step of receiving the connection information (control data D) supplied from the upper layer controller 40 before switching, and the same after switching, respectively (Column 6 Line 45-49); an information writing step of writing the connection information (control data D) for use after switching all of the connection information received in the information receiving step (Column 5 Line 31-34), when a switching request (write control signal 306) is delivered from the side of the upper layer 40; a switching signal generation step of generating a switching signal (WS and SE in Column 5 Line 40-41) for switching in synchronization with the timing (Column 4 Line 38-39) in response to the switching directive (write control signal 306) of the connection information received from the upper layer controller 40; a copying step of reading out the connection information (control data D) after switching on a rising edge of the switching signal generated in the switching signal generation step as the connection information before switching (Column 5 Line 25-33); a read-out step of storing the connection information (control data D) as read out in the copying step (Column 5 Line 31-34), and reading out the multiplexed data as written in the

writing step on the basis of the connection information (Column 1 Line 18-30); and a selection step of selecting the connection information (control data D) in response to a fall of the switching signal generated (Column 5 Line 67 – Column 6 Line 2).

Regarding to claim 8, Masuda teaches wherein the copying step reads out addresses and data contained in the connection information (control data D) written in the information writing step, in increasing address order, supplying the same to the read-out step, and the read-out step writes data of connection information, as supplied, to an address (address signal ADR) indicated by the connection information, as supplied, while reading out the data written in increasing address order; and using the data as read-out addresses for the data of the time slots written in the writing step (Column 1 Line 26-30).

Response to Arguments

3. Applicant's arguments filed on August 17, 2005 have been fully considered but they are not persuasive.

There is no argument regarding to claims 5-8.

Allowable Subject Matter

4. Claim 1-4, 9 and 10 are allowed.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clemence Han whose telephone number is (571) 272-3158. The examiner can normally be reached on Monday-Thursday 7 - 5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571) 272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

C. H.

Clemence Han
Examiner
Art Unit 2665

STEVEN NGUYEN
PRIMARY EXAMINER